CLAIMS

What is claimed is:

1. An on-chip multiple tap transformer balun comprises:

first winding operably coupled for a single-ended signal;

first portion of a second winding, wherein a first node of the first portion of the second winding is operably coupled for a first leg of a first differential signal, wherein a second node of first portion of the second winding is operably coupled to a reference potential, and wherein a tap of the first portion of the second winding is operably coupled for a first leg of a second differential signal; and

second portion of the second winding, wherein a first node of the second portion of the second winding is operably coupled for a second leg of the first differential signal, wherein a second node of the second portion of the second winding is operably coupled to the reference potential, wherein a tap of the second portion of the second winding is operably coupled for a second leg of the second differential signal, wherein the second portion of the second winding is substantially symmetrical to the first portion of the second winding, and wherein the tap of the first portion of the second winding is substantially symmetrical to the tap of the second portion of the second winding.

2. The on-chip multiple tap transformer balun of claim 1, wherein each of the first and second portions of the second winding further comprises a substantially octagon interwound shape.

3. The on-chip multiple tap transformer balun of claim 1 further comprises

a shunt winding on a third layer of the integrated circuit, wherein the shunt winding is coupled in parallel with the first winding.

4. The on-chip multiple tap transformer balun of claim 1 further comprises:

the first portion of the second winding including a second tap operably coupled for a first leg of a third differential signal; and

the second portion of the second winding including a second tap operably coupled for a second leg of the third differential signal, wherein the second tap of the first portion is symmetrical to the second tap of the second portion.

5. The on-chip multiple tap transformer balun of claim 1 further comprises:

a shunt winding on a third layer of the integrated circuit, wherein the shunt winding is connected in parallel to with the second winding.

6. The on-chip multiple tap transformer balun of claim 1, wherein the second layer further comprises a metalization layer of the integrated circuit having lowest resistivity.

7. The on-chip multiple tap transformer balun of claim 1, wherein the first winding further comprises multiple turns.

8. The on-chip multiple tap transformer balun of claim 1, wherein the second winding further comprises multiple turns.

9. The on-chip multiple tap transformer balun of claim 1, wherein the second winding further comprises:

a rectangular octagonal shape having a first dimension lengthened with respect to a square octagonal reference shape and having a second dimension shortened with respect to the square octagonal reference shape, wherein area of the rectangular octagonal shape is similar to area of the square octagonal reference shape.

10. The on-chip multiple tap transformer balun of claim 1 further comprises:

an integrated circuit size based on a balancing of inductance values of the on-chip multiple tap transformer balun, turns ratio of the on-chip multiple tap transformer balun, quality factor of the on-chip multiple tap transformer balun, and capacitance of the on-chip multiple tap transformer balun.